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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/711,795 | 10/06/2004 | Chun-Yang Lin | ACMP0164USA | 5794 |

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| EXAMINER | |
|---|---|
| PATEL, ISHWARBHAI B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2841 | |

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/711,795 | LIN ET AL. | |
| | Examiner | Art Unit | |
| | Ishwar (I. B.) Patel | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☐ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is in response to amendment filed on February 22, 2006.

### *Drawings*

2. The amended figure filed on February 22, 2006 is not accepted because of the following informalities.

Structure of the pseudo layout as shown in old figure 5 and as described in the specification is a net like structure. The old figure 5 can be amended by just providing a different shading instead of the cross-hatching pattern. The amended figure 5 shows islands, which appear, not to be correct.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Asai (US Patent No. 6,392,898).

**Regarding claim 1**, Asai, in figure 1, discloses a multi-layer printed circuit board (PCB) comprising: a plastic substrate containing a plurality of layers (plurality of insulating layers, 30, 50, 70, see figure 1); and a circuit layout formed on at least one layer of the plastic substrate, the circuit layout having a first layout (58U) and a second layout (58M), wherein the second layout comprises a pseudo-layout (dummy pattern, column 6,line 12-20) to prevent the PCB from being bent when heated (column 12, line 17-25).

**Regarding claim 2**, Asai further discloses density of circuits of the second layout has a lower circuit density than that of the first layout (more circuit lines on the layer than the dummy line 58M, see figure 1).

**Regarding claim 3**, Asai further discloses the circuit layout comprises signal traces and power traces, the pseudo-layout is isolated from the signal traces and the power traces on the PCB (column 6, line 13-53).

**Regarding claim 4**, Asai further discloses the pseudo-layout comprises a plurality of pseudo-traces (58M) neither for power nor signal transmission (column 6, line 45-53).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai, as applied to claim 1 above, and further in view of Valluri (US Patent No. 6,507,100).

**Regarding claim 5**, Asai discloses all the features of the claimed invention including the pseudo-traces as applied to claim 1 above but does not disclose the pseudo-traces are parallel to each other in a netlike structure. Valluri, in figure 3 and 5, discloses functional pattern (31,32) and non-functional (dummy) pattern with net like structure (33, detail shown in figure 5) and further recites that the dummy patterns have a width of about 70 to 100 μm and a spacing of about 80 μm to 300 μm (3.12 mil to 11.7

mil) to balance metallization to reduce warpage and bending of the board (column 5, line 13-30).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the pseudo-traces of Asai with the netlike structure, as taught by Valluri, in order to optimize the balancing of the metallization to reduce warpage and bending of the board.

**Regarding claim 6-7**, the modified circuit board of Asai discloses all the features of the claimed invention as applied to claim 5 above but does not disclose the interval distance is 5 mil as claimed in claim 6 and the width of the pseudo-traces is 5 mil, as claimed in claim 7. As applied to claim 5 above, Valluri discloses the dummy patterns in net-like structure with a width of about 70 to 100 μm and a spacing of about 80 μm to 300 μm (3.12 mil to 11.7 mil) to balance metallization to reduce warpage and bending of the board (column 5, line 13-30)

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to select the interval and width of the pseudo-traces (dummy pattern) to have desired balance of metallization to reduce warpage and bending of the board.

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the structure of Asai with the

limitations as claimed in claims 6 and 7, as taught by Valluri, in order to balance metallization to reduce warpage and bending of the board.

7. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent No. 6,534,852) in view of admitted prior art figure 2 and 3 (APA).

**Regarding claim 1**, Lin, in figure 3, discloses a printed circuit board (PCB) comprising: a plastic substrate (302); and a circuit layout formed on the plastic substrate, having a first layout (309, 307) and a second layout (306), wherein the second layout comprises a pseudo-layout to prevent the PCB from being bent when heated. Lin does not disclose a multilayer printed circuit board with plurality of layers. Lin discloses only one layer of substrate. However, multilayer substrate with plurality of plastic layers is known in the art for increasing the component density and better routing of the traces. APA discloses one such multilayer circuit board with first and second layout. A person of ordinary skill in the art would be motivated to provide the circuit board of Lin with plurality of plastic layers to increase the component density and better routing of the traces in the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Lin with plurality of plastic layers, from the teachings of APA, in order to have a circuit board with increased component density and facilitating better routing of the traces in the board.

**Regarding claim 2**, the modified board of Lin further discloses density of circuits of the second layout has a lower circuit density than that of the first layout (see figure 3).

**Regarding claim 3**, the modified board of Lin further discloses the circuit layout comprises signal traces and power traces (309,307), the pseudo-layout is isolated from the signal traces and the power traces on the PCB (306 is isolated from 309,307).

**Regarding claim 4**, the modified board of Lin further discloses the pseudo-layout comprises a plurality of pseudo-traces (306) neither for power nor signal transmission.

**Regarding claim 5**, the modified board of Lin further discloses the pseudo-traces are parallel to each other in a netlike structure (306, net like structure and traces parallel to each other).

8. Claims 6 and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over the modified board of Lin as applied to claim 1 above, and further in view of Valluri (US Patent No. 6,507,100).

**Regarding claims 6 and 7**, the modified board of Lin discloses all the features of the claimed invention including the netlike structure of the parallel pseudo-traces having an interval distance as applied to claim 5 above, but does disclose the interval distance is 5 mil as claimed in claim 6 and the width of the pseudo-traces is 5 mil, as claimed in

claim 7. Lin discloses the interval distance of 200 μm (about 8 mil) and width of the pseudo-traces as 100 μm (3.9 mil).

Valluri, in figure 3 and 5, discloses functional pattern (31,32) and non-functional (dummy) pattern (33, detail shown in figure 5) and further recites that the dummy patterns have a width of about 70 to 100 μm and a spacing of about 80 μm to 300 μm (3.12 mil to 11.7 mil) to balance metallization to reduce warpage and bending of the board (column 5, line 13-30).

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to select the interval and width of the pseudo-traces (dummy pattern) to have desired balance of metallization to reduce warpage and bending of the board.

Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Lin with the limitations as claimed in claims 6 and 7, in order to balance metallization to reduce warpage and bending of the board.

***Response to Arguments***

9. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoneda (US Patent No. 6,717,069), in figure 16, discloses a circuit board with plurality of plastic layers and pseudo trace (dummy member 46) in to equalize density of wiring lines (column 10, line 19-29).

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Patent Examiner
Art Unit: 2841
April 24, 2006

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